2011년2학기
임베디드시스템 응용(#514118)
#11. Serial communication 5
I²C-bus, IIC0 #2

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Configuration of IIC0

Table 18-1. Configuration of Serial Interface IIC0

Item	Configuration
Registers	IIC shift register 0 (IIC0) Slave address register 0 (SVA0)
Control registers	IIC control register 0 (IICC0) IIC status register 0 (IICS0) IIC flag register 0 (IICF0) IIC clock selection register 0 (IICCL0) IIC function expansion register 0 (IICX0) Port mode register 6 (PM6) Port register 6 (P6)

7bit addressing support only.

Port seutp

- SCL0: P6.0
- SDA0: P6.1
- PM6.x=0
- P6.x=0

(Set IICE0=1 before port setup)

Control regs.: IICC0

- IIC control register 0 (IICC0)

Figure 18-5. Format of IIC Control Register 0 (IICC0) (1/4)

Address: FFA6H After reset: 00H R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
IICC0	IICE0	LREL0	WREL0	SPIE0	WTIM0	ACKE0	STT0	SPT0

- IICE0: en/disable module
- LREL0: 현재 통신 동작 취소하고 대기 상태로 만듬.
- WREL0: wait 취소
- SPIE0: Stop condition 발견 시 인터럽트 발생 유무 결정
- WTIM0: wait 시점 결정 (8/9번째 클럭)
- ACKE0: ACK 제어 (en/disable)
- STT0: Start condition trigger
- SPT0: Stop condition trigger

Control regs.: IICCL0

- IIC clock selection reg.0 (IICCL0)

Figure 18-8. Format of IIC Clock Selection Register 0 (IICCL0)

Address: FFA8H After reset: 00H R/W[Note]

Symbol	7	6	<5>	<4>	<3>	<2>	1	0
IICCL0	0	0	CLD0	DAD0	SMC0	DFC0	CL01	CL00

Read only

- SMC0: standard/high-speed mode 결정
  - Standard: 0~100KHz, high-speed:~400KHz
- DFC0: digital filter on/off in high-speed mode
- Clock speed selection:

Table 18-2. Selection Clock Setting

IICX0	IICCL0			Selection Clock (fw)	Transfer Clock (fw/m)	Settable Selection Clock (fw) Range	Operation Mode
Bit 0	Bit 3	Bit 1	Bit 0				
CLX0	SMC0	CL01	CL00				
0	0	0	0	$f_{PRS}/2$	fw/44	2.00 to 4.19 MHz	Normal mode (SMC0 bit = 0)
0	0	0	1	$f_{PRS}/2$	fw/86	4.19 to 8.38 MHz	
0	0	1	0	$f_{PRS}/4$	fw/86		
0	0	1	1	f_{EXSCL0}	fw/66	6.4 MHz	
0	1	0	×	$f_{PRS}/2$	fw/24	4.00 to 8.38 MHz	High-speed mode (SMC0 bit = 1)
0	1	1	0	$f_{PRS}/4$	fw/24		
0	1	1	1	f_{EXSCL0}	fw/18	6.4 MHz	
1	0	×	×	Setting prohibited			
1	1	0	×	$f_{PRS}/2$	fw/12	4.00 to 4.19 MHz	High-speed mode (SMC0 bit = 1)
1	1	1	0	$f_{PRS}/4$	fw/12		
1	1	1	1	Setting prohibited			

Control regs.: IICS0

- IIC status registers (IICS0)

Figure 18-6. Format of IIC Status Register 0 (IICS0) (1/3)

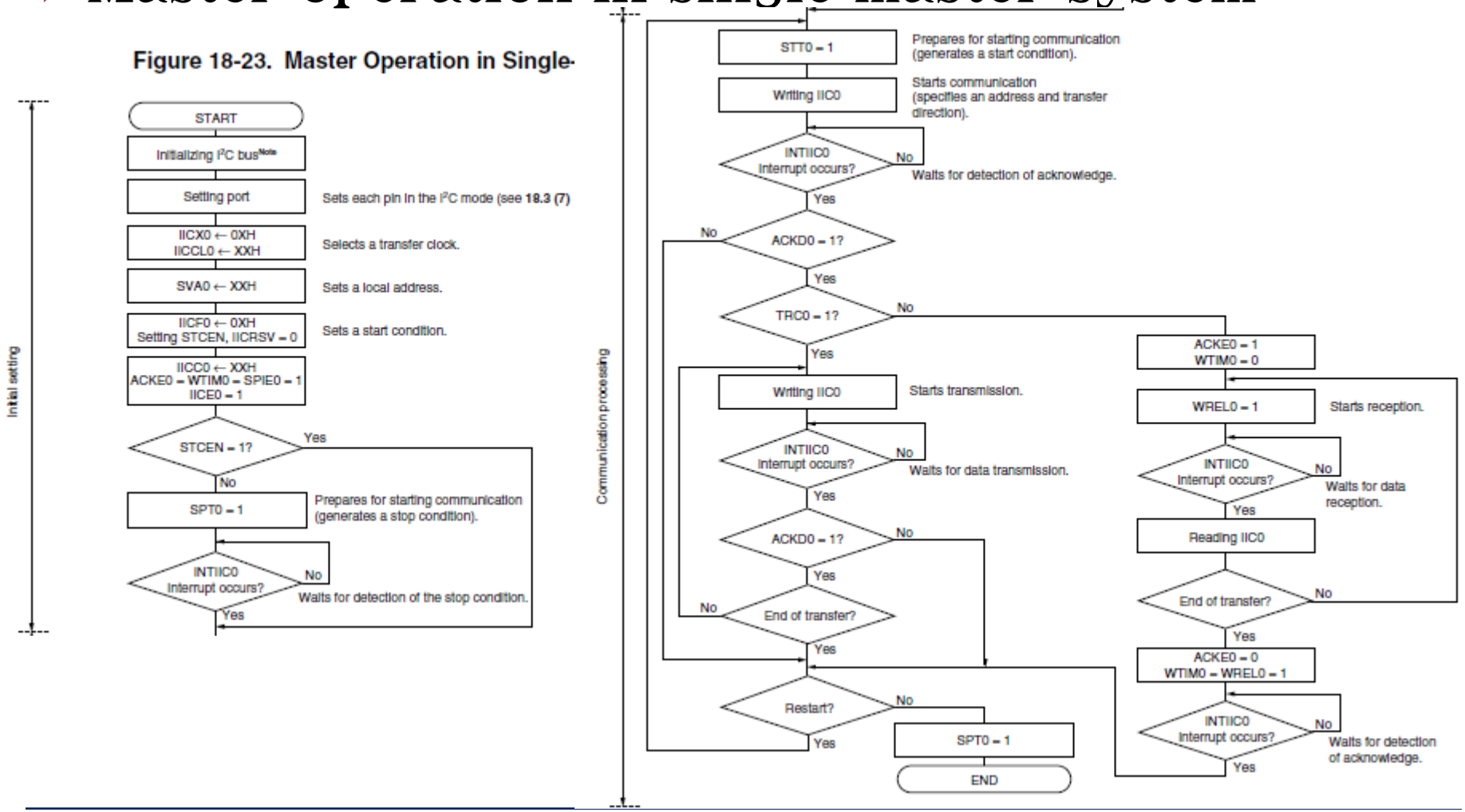
Address: FFAAH After reset: 00H R

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
IICS0	MSTS0	ALD0	EXC0	COI0	TRC0	ACKD0	STD0	SPD0

- MSTS0: master(1),slave/통신대기 상태(0)
- ALD0: arbitration loss, 1:loss, 0:win
- EXC0: detection of extension code (10bit add.)
- COI0: detection of matching add.
- TRC0: detection of tx/tx status, 0:rx, 1:tx
- ACKD0: detection of ack. (nACK)
- STD0: detection of start cond.
- SPD0: detection of stop cond.

Operations: master

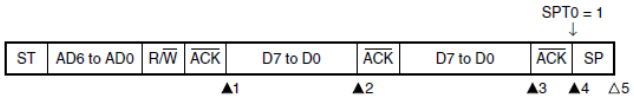
- Master operation in single master system



Timing of INTIIC0

(a) Start ~ Address ~ Data ~ Data ~ Stop (transmission/reception)

(i) When WTIM0 = 0

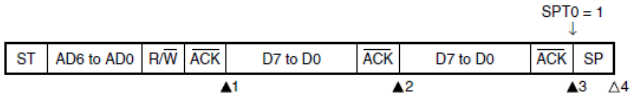


▲1: IICS0 = 1000×110B
▲2: IICS0 = 1000×000B
▲3: IICS0 = 1000×000B (Sets WTIM0 to 1)[Note]
▲4: IICS0 = 1000××00B (Sets SPT0 to 1)[Note]
△5: IICS0 = 00000001B

Note To generate a stop condition, set WTIM0 to 1 and change the timing for generating the INTIIC0 interrupt request signal.

Remark ▲: Always generated
△: Generated only when SPIE0 = 1
×: Don't care

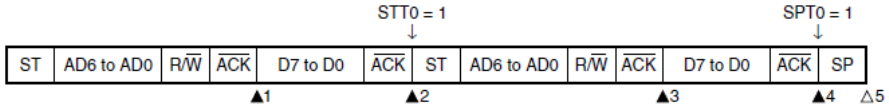
(ii) When WTIM0 = 1



▲1: IICS0 = 1000×110B
▲2: IICS0 = 1000×100B
▲3: IICS0 = 1000××00B (Sets SPT0 to 1)
△4: IICS0 = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE0 = 1
×: Don't care

Restart



▲1: IICS0 = 1000×110B
▲2: IICS0 = 1000××00B (Sets STT0 to 1)
▲3: IICS0 = 1000×110B
▲4: IICS0 = 1000××00B (Sets SPT0 to 1)
△5: IICS0 = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE0 = 1
×: Don't care

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Operations

- Slave opeartion
  - Event-driven
  - Flags
    - communication mode flag
    - ready flag
    - comm. direction flag

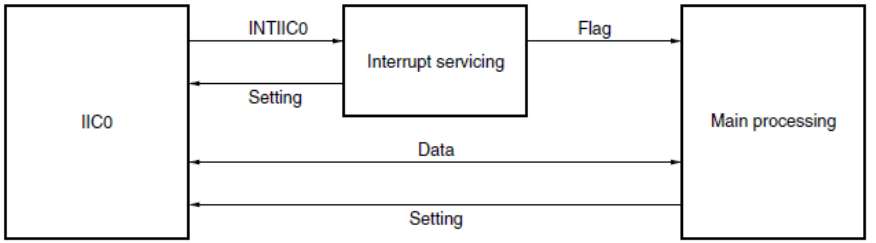
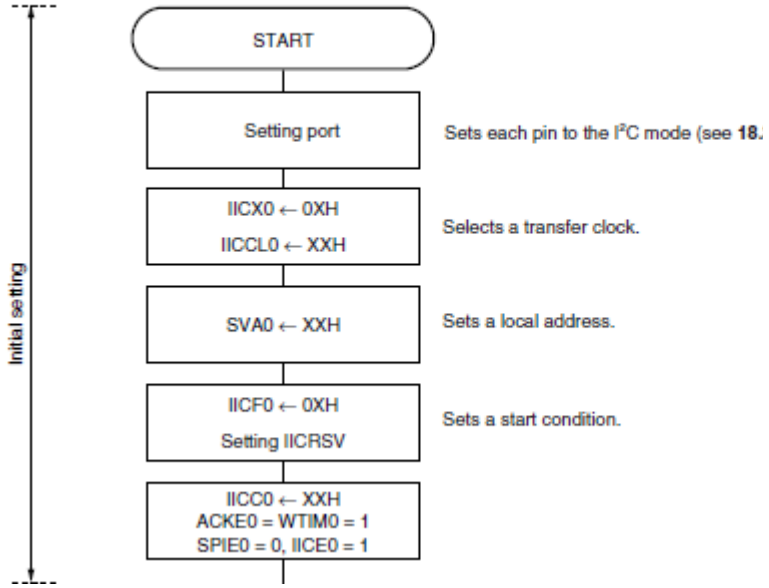
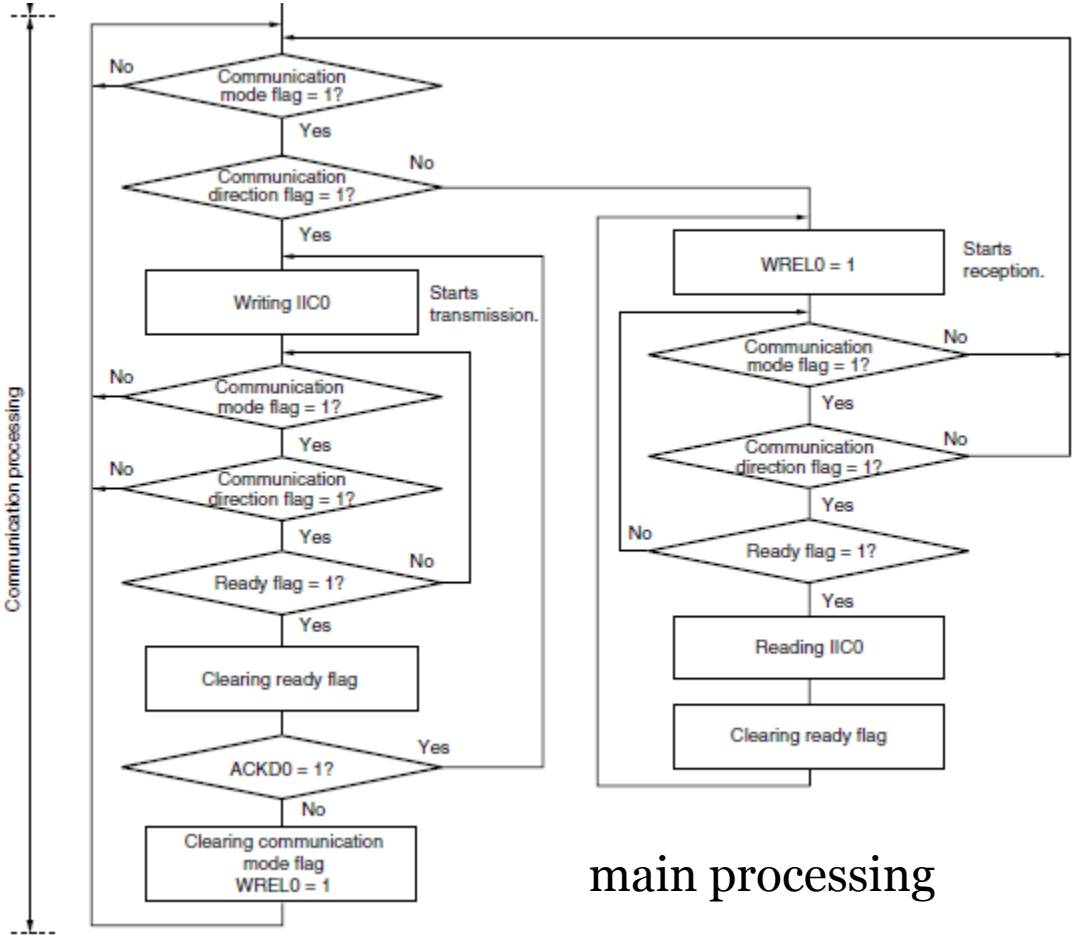


Figure 18-25. Slave Operation Flowcha



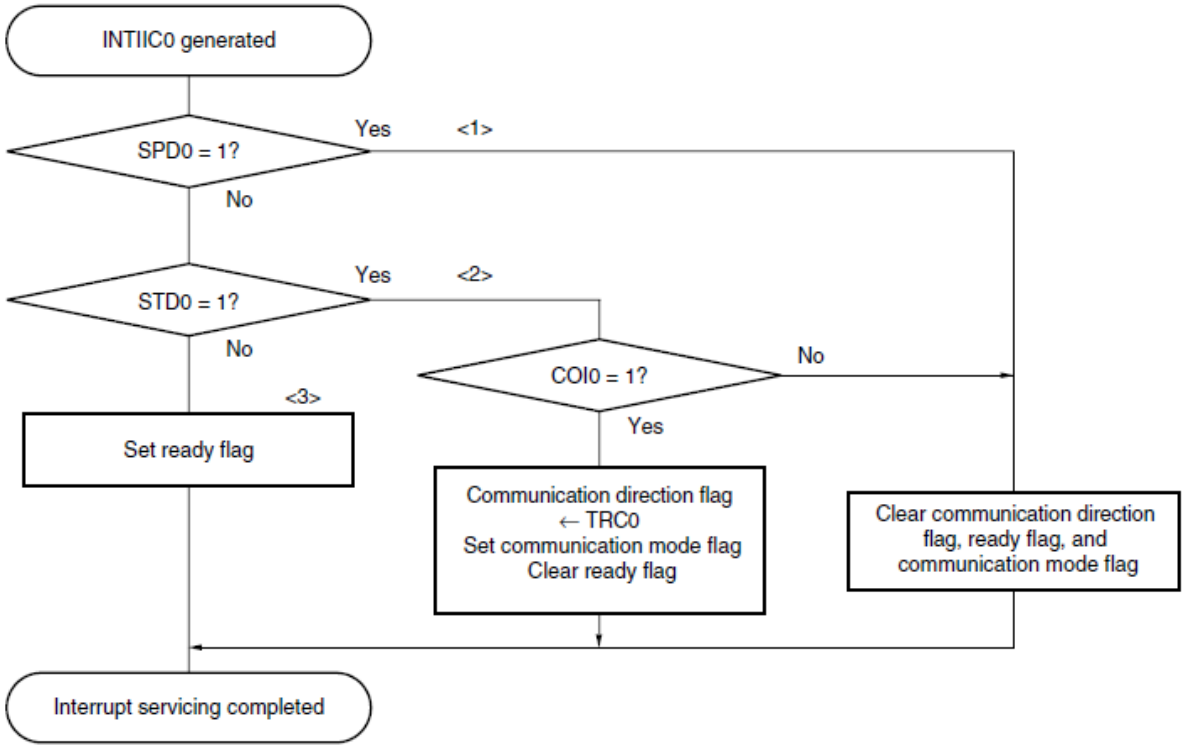


main processing

Operations

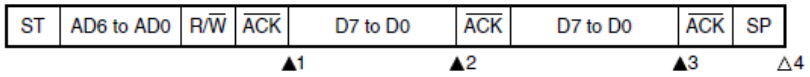
- Slave operation: ISR

Figure 18-26. Slave Operation Flowchart (2)



Timing of INTIIC0

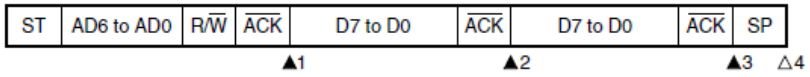
(i) When WTIM0 = 0



▲1: IICS0 = 0001×110B
▲2: IICS0 = 0001×000B
▲3: IICS0 = 0001×000B
△4: IICS0 = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE0 = 1
×: Don't care

(ii) When WTIM0 = 1



▲1: IICS0 = 0001×110B
▲2: IICS0 = 0001×100B
▲3: IICS0 = 0001××00B
△4: IICS0 = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE0 = 1
×: Don't care

Code for IIC0 master operation

```
unsigned char txflag;
#pragma vect INTIIC0 i2c_isr
__interrupt void i2c_isr(void)
{
   if(!send_end) {
         //prepare tx data
         txdata=DATA_TX;
         IIC0 = txdata;
   }
   else
         SPT0 = 1;
}
void main(void)
{
    //first enable IIC0 module
    IICC0 = 0x80;
    //port setup for IIC0
    PM6.0 = 0, PM6.1 = 0;
    P6.0 = 0, P6.1 = 0;
    //setup IIC0
    //set clock selection
    IICX0 = 0;
    IICCL0 = 0x02; //fPRS/4, fw/86
    SVA0 = I2CADD_ME;
    IICF0 = 0x02;  //STCEN=1
    IICC0 = 0x9c;  //IICE0, SPIE0,
WTIM0, ACKE0=1

        IICMK0 = 0;
        EI();

        //send start cond.
        STT0 = 1;
        //send slave add. + nWrite
        IIC0 = I2CADD_SLAVE;

}
```