임베디드시스템 기초(#514115)

#9. Analog-Digital Converter 1/2

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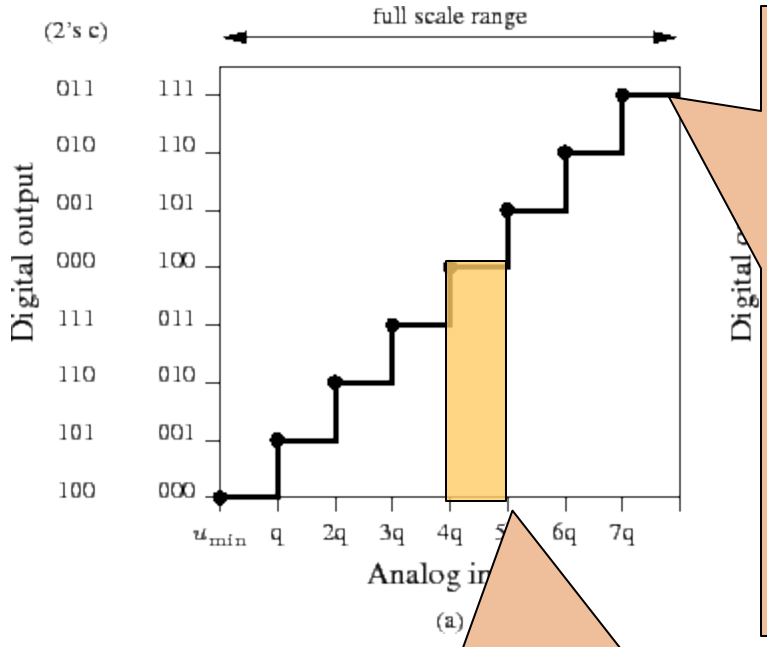
Contents

- Analog to Digital Converter
  - Ideal and Real ADC
  - MSP430 ADC12
    - Features
    - Block diagram
    - Operation
    - Control registers

Ideal ADC

- 3-bit ADC



Transfer function of N-bit ADC (전달함수)

$$N_{ADC} = \text{nint}(2^N \frac{V_{in}}{V_{FS}})$$

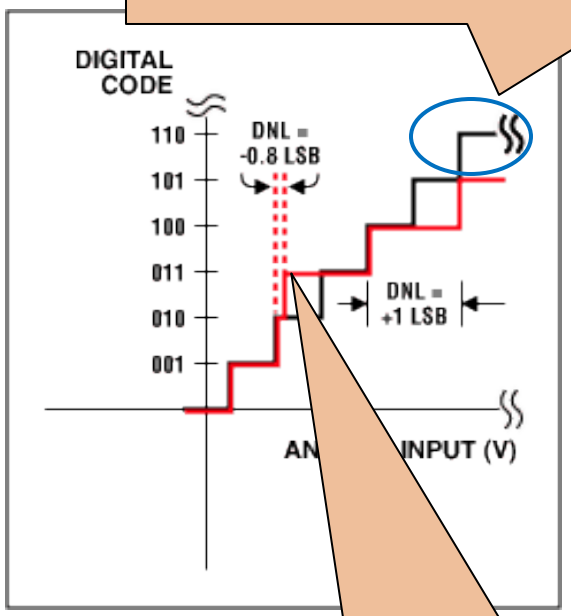
nint() 함수는 인자 값과 가장 가까운 정수를 출력.
출력은 0~2^N −1 범위

이 범위 내 입력 값은 모두 100 출력 값. → 1LSB = $V_{FS}/8$

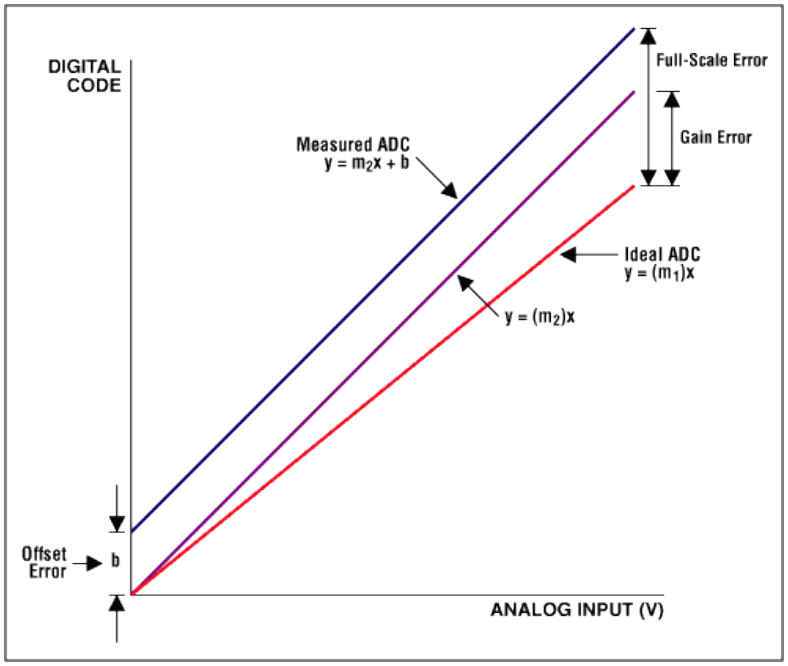
Real ADC

- 이상적인 ADC와 달리 불완전한 특성을 가짐.

Missing code: 110 code를 만드는 입력이 없음.



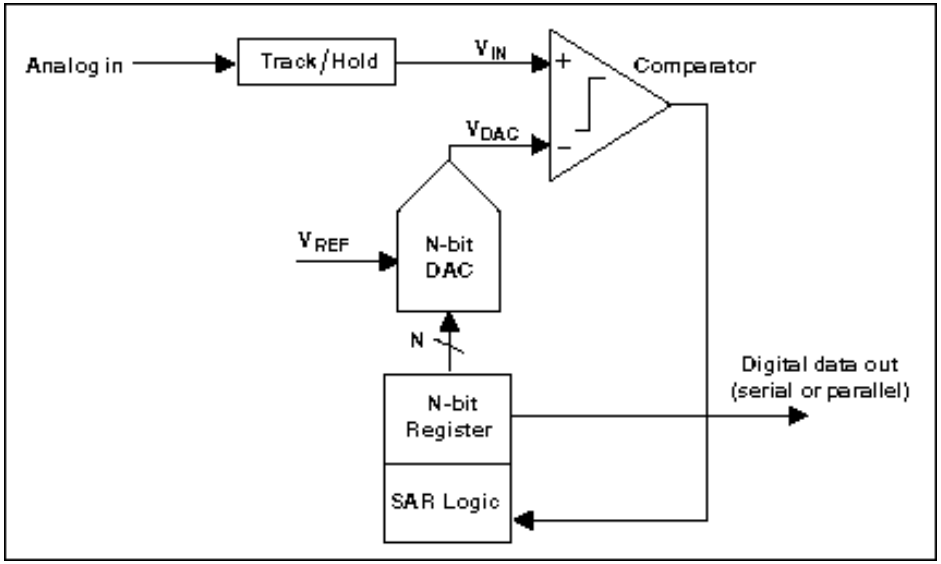
Differential nonlinearity(DNL): 모든 step이 1LSB 폭을 유지해야 하나 달라짐.

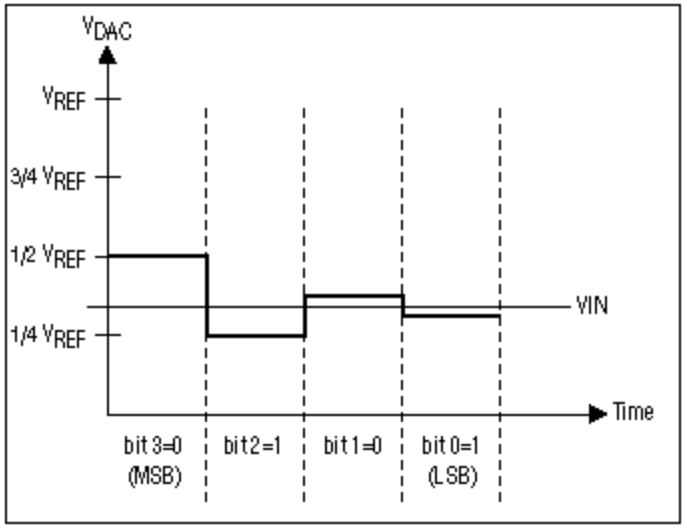


➔Total unadjusted error (maximum deviation between ideal and real ADC): Ex. ±2LSB (typical, ±5LSB max.) in MSP430 datasheet

SAR ADC 작동 원리

- Successive-approximation-register (SAR) analog-to-dig ital converters (ADCs)

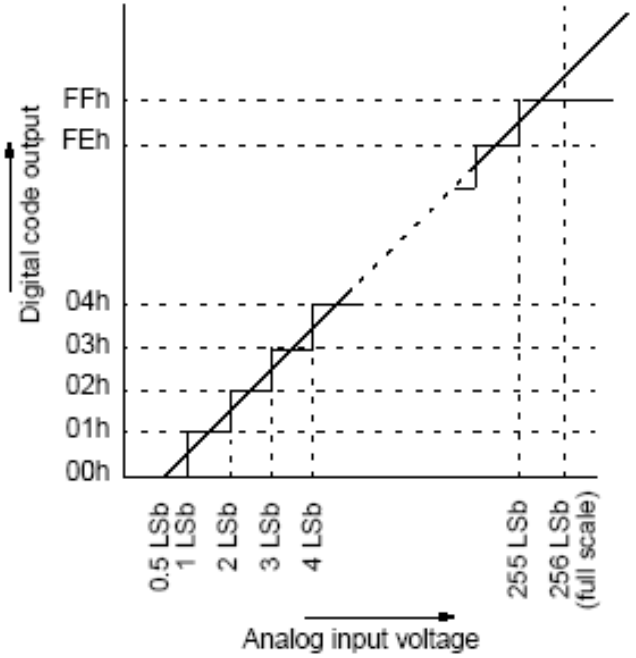




ADC에서의 중요 특성

- Sample rate: samples per second (SPS),즉, 얼마나 자주 신호를 변환할 것인가를 나타내는 숫자
- Resolution: 각 샘플의 정확도 지칭
  - 예: 8-bit ADC (0~255) 256 단계, 10-bit ADC (0~1023) 1024 단계로 보다 세밀하게 구분 가능

이상적인 ADC 특성



MSP430 ADC12 features

ADC12 features include:

- Greater than 200-ksps maximum conversion rate
- Monotonic 12-bit converter with no missing codes
- Sample-and-hold with programmable sampling periods controlled by software or timers.
- Conversion initiation by software, Timer_A, or Timer_B
- Software selectable on-chip reference voltage generation (1.5 V or 2.5 V)
- Software selectable internal or external reference
- Eight individually configurable external input channels (twelve on MSP430FG43x and MSP430FG461x devices)
- Conversion channels for internal temperature sensor, AV_{CC}, and external references
- Independent channel-selectable reference sources for both positive and negative references
- Selectable conversion clock source
- Single-channel, repeat-single-channel, sequence, and repeat-sequence conversion modes
- ADC core and reference voltage can be powered down separately
- Interrupt vector register for fast decoding of 18 ADC interrupts
- 16 conversion-result storage registers

- ksps: kilo samples per second

- 변환시작 by 소프트웨어, TA, TB
- 기준전압발생기 내장→ 1.5V, 2.5V
- 내/외부 기준전압 선택가능

- 내부 온도센서, Avcc, 외부 기준전압용 채널 제공
- 각 채널 별로 기준전압 설정 가능

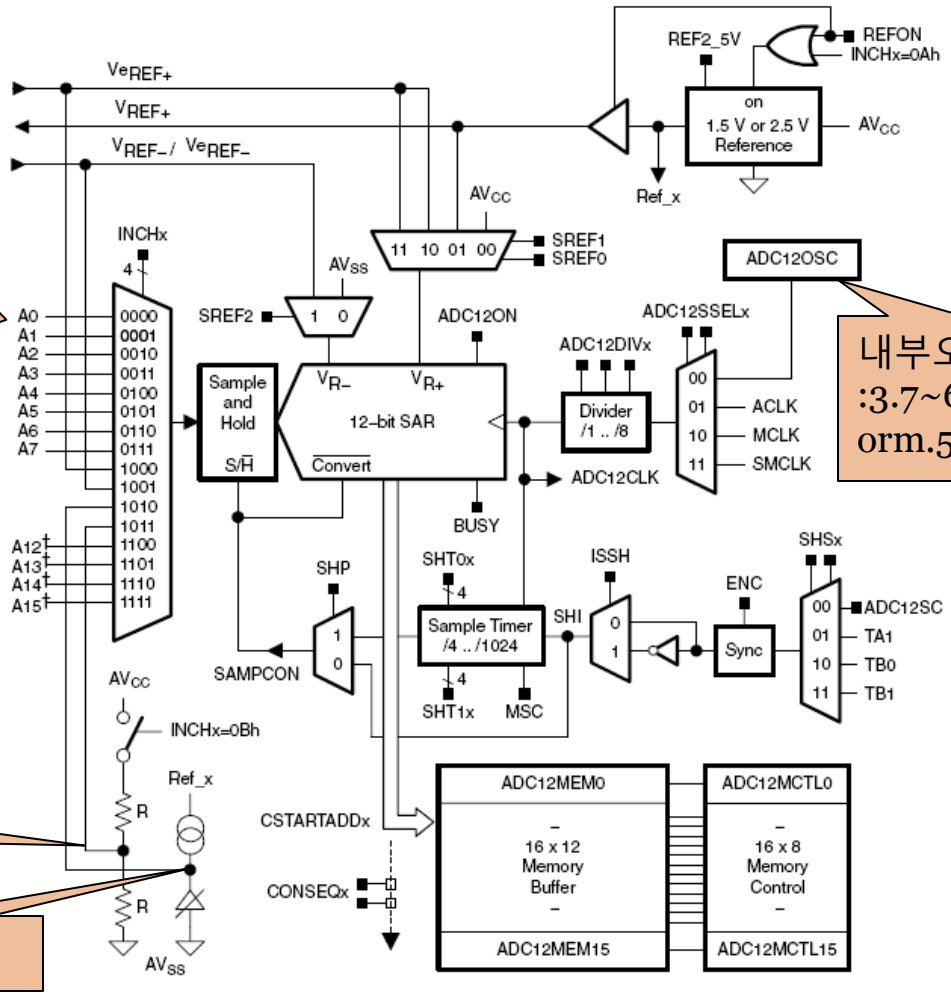
- 변환 클럭 소스(4가지) 선택 가능
- **단일채널,** 단일채널반복, 일정순서, 순서반복 변환 기능 제공

- 18개 인터럽트 사건 발생, ADC 별도 벡터 제공
- 16개 변환결과 레지스터 제공

ADC12 block diagram

Figure 26–1. ADC12 Block Diagram

8개의 아날로그 입력 채널(A0~A7)+4개의 내부 입력(VeRef+/-,Avcc/2, Temp. sensor)
*4개 추가 채널(A12~15, 43x/461x only)



내부오실레이터 :3.7~6.3MHz(norm.5MHz)

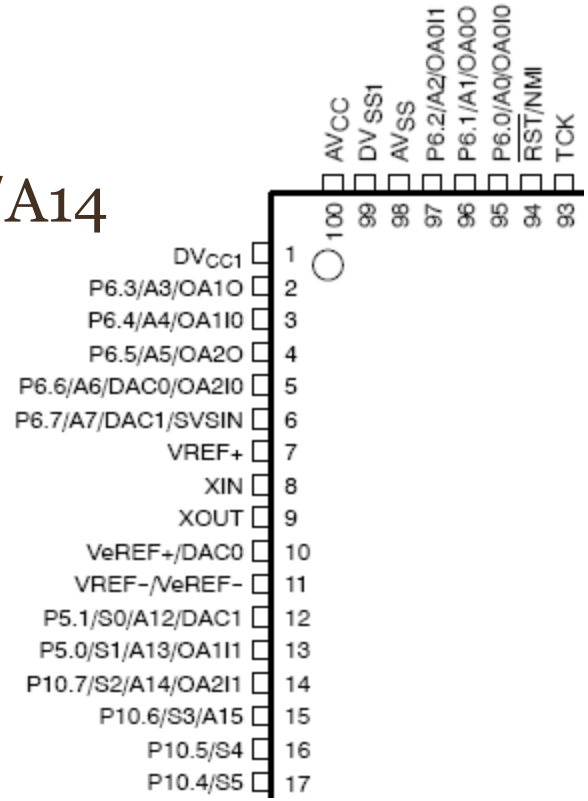
Avcc/2 입력

내부온도센서

† MSP430FG43x and MSP430FG461x devices only

ADC12 Pin 배치

- 모두 16개 핀과 연결
  - P6.0/A0 ~P6.7/A7
  - VREF+, VeREF+, VREF-/VeREF-
  - P5.1/A12, P5.0/A13, P10.7/A13, P10.6/A14
- 전달함수
  - $N_{ADC} = 4095*(V_{IN} – V_{R-})/(V_{R+} - V_{R-})$



관련 SFRs

Table 26–2. ADC12 Registers

Register	Short Form	Register Type	Address	Initial State
ADC12 control register 0	ADC12CTL0	Read/write	01A0h	Reset with POR
ADC12 control register 1	ADC12CTL1	Read/write	01A2h	Reset with POR
ADC12 interrupt flag register	ADC12IFG	Read/write	01A4h	Reset with POR
ADC12 interrupt enable register	ADC12IE	Read/write	01A6h	Reset with POR
ADC12 interrupt vector word	ADC12IV	Read	01A8h	Reset with POR
ADC12 memory 0	ADC12MEM0	Read/write	0140h	Unchanged
ADC12 memory 1	ADC12MEM1	Read/write	0142h	Unchanged
...				
ADC12 memory 15	ADC12MEM15	Read/write	015Eh	Unchanged
ADC12 memory control 0	ADC12MCTL0	Read/write	080h	Reset with POR
ADC12 memory control 1	ADC12MCTL1	Read/write	081h	Reset with POR
ADC12 memory control 2	ADC12MCTL2	Read/write	082h	Reset with POR
ADC12 memory control 3	ADC12MCTL3	Read/write	083h	Reset with POR
...				
ADC12 memory control 14	ADC12MCTL14	Read/write	08Eh	Reset with POR
ADC12 memory control 15	ADC12MCTL15	Read/write	08Fh	Reset with POR

전체 동작 제어, 중요!

인터럽트 관련

변환결과값
16개 메모리

각각의 메모리별로 설정함. 입력, 기준전압 등 설정

ADC12CTL0: ADC12 control reg. 0

ADC12CTL0, ADC12 Control Register 0

15	14	13	12	11	10	9	8
SHT1x				SHT0x			
rw–(0)	rw–(0)	rw–(0)	rw–(0)	rw–(0)	rw–(0)	rw–(0)	rw–(0)

7	6	5	4	3	2	1	0
MSC	REF2_5V	REFON	ADC12ON	ADC12OVIE	ADC12 TOVIE	ENC	ADC12SC
rw–(0)	rw–(0)	rw–(0)	rw–(0)	rw–(0)	rw–(0)	rw–(0)	rw–(0)

Modifiable only when ENC = 0

SHT1x Bits 15-12 Sample-and-hold time. These bits define the number of ADC12CLK cycles in the sampling period for registers ADC12MEM8 to ADC12MEM15.

SHT0x Bits 11-8 Sample-and-hold time. These bits define the number of ADC12CLK cycles in the sampling period for registers ADC12MEM0 to ADC12MEM7.

SHTx Bits	ADC12CLK cycles
0000	4
0001	8
0010	16
0011	32
0100	64
0101	96
0110	128
0111	192
1000	256
1001	384
1010	512
1011	768
1100	1024
1101	1024
1110	1024
1111	1024

샘플링 시간 간격 설정. 즉, 내부 커패시터를 충전 시키는 시간임.
-너무 짧으면 입력 전압 보다 작은 전압 값으로 변환.
-너무 느리면 전체 변환 시간이 느려짐.
-16개 메모리를 2개 그룹(0~7,8~15)으로 나누어 결정함.

MSC Bit 7 Multiple sample and conversion. Valid only for sequence or repeated modes.
0 The sampling timer requires a rising edge of the SHI signal to trigger each sample-and-conversion.
1 The first rising edge of the SHI signal triggers the sampling timer, but further sample-and-conversions are performed automatically as soon as the prior conversion is completed.

REF2_5V Bit 6 Reference generator voltage. REFON must also be set.
0 1.5 V
1 2.5 V

REFON Bit 5 Reference generator on
0 Reference off
1 Reference on

ADC12ON Bit 4 ADC12 on
0 ADC12 off
1 ADC12 on

ADC12OVIE Bit 3 ADC12MEMx overflow-interrupt enable. The GIE bit must also be set to enable the interrupt.
0 Overflow interrupt disabled
1 Overflow interrupt enabled

ADC12 TOVIE Bit 2 ADC12 conversion-time-overflow interrupt enable. The GIE bit must also be set to enable the interrupt.
0 Conversion time overflow interrupt disabled
1 Conversion time overflow interrupt enabled

ENC Bit 1 Enable conversion
0 ADC12 disabled
1 ADC12 enabled

ADC12SC Bit 0 Start conversion. Software-controlled sample-and-conversion start. ADC12SC and ENC may be set together with one instruction. ADC12SC is reset automatically.
0 No sample-and-conversion-start
1 Start sample-and-conversion

ADC12CTL1: ADC12 control reg. 1

ADC12CTL1, ADC12 Control Register 1

15	14	13	12	11	10	9	8
CSTARTADDx				SHSx		SHP	ISSH
rw–(0)	rw–(0)	rw–(0)	rw–(0)	rw–(0)	rw–(0)	rw–(0)	rw–(0)

7	6	5	4	3	2	1	0
ADC12DIVx			ADC12SSELx		CONSEQx		ADC12 BUSY
rw–(0)	rw–(0)	rw–(0)	rw–(0)	rw–(0)	rw–(0)	rw–(0)	r–(0)

Modifiable only when ENC = 0

CSTARTADDx Bits 15-12 Conversion start address. These bits select which ADC12 conversion-memory register is used for a single conversion or for the first conversion in a sequence. The value of CSTARTADDx is 0 to 0Fh, corresponding to ADC12MEM0 to ADC12MEM15.

SHSx Bits 11-10 Sample-and-hold source select
- 00 ADC12SC bit
- 01 Timer_A.OUT1
- 10 Timer_B.OUT0
- 11 Timer_B.OUT1

SHP Bit 9 Sample-and-hold pulse-mode select. This bit selects the source of the sampling signal (SAMPCON) to be either the output of the sampling timer or the sample-input signal directly.
- 0 SAMPCON signal is sourced from the sample-input signal.
- 1 SAMPCON signal is sourced from the sampling timer.

ISSH Bit 8 Invert signal sample-and-hold
- 0 The sample-input signal is not inverted.
- 1 The sample-input signal is inverted.

ADC12DIVx Bits 7-5 ADC12 clock divider
- 000 /1
- 001 /2
- 010 /3
- 011 /4
- 100 /5
- 101 /6
- 110 /7
- 111 /8

ADC12CLK 주파수 결정

16개 메모리중 어떤 것을 사용할지를 결정!
싱글채널 단일변환 시는 대개 메모리 하나만 사용!

ADC12CTL0의 SHT0/1에 따라 이 간격 결정!

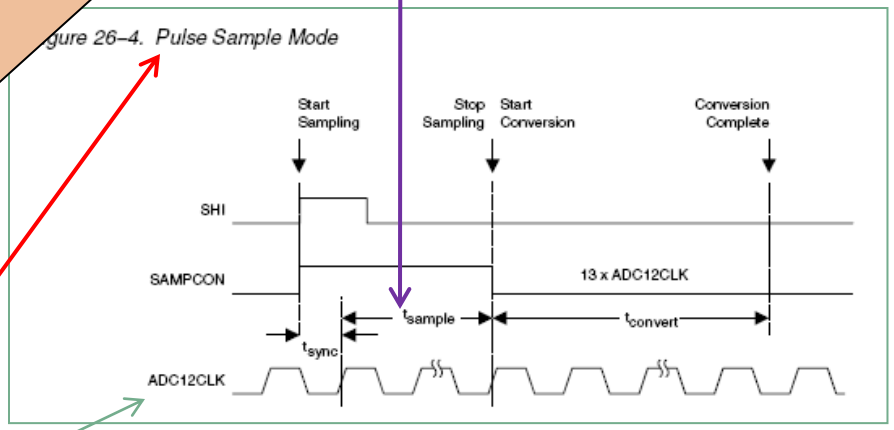


Figure 26–4. Pulse Sample Mode

ADC12SSELx Bits 4-3 ADC12 clock source select
- 00 ADC12OSC
- 01 ACLK
- 10 MCLK
- 11 SMCLK

변환방법 설정!
싱글채널 단일변환만 공부함.
(CONSEQ:00)

CONSEQx Bits 2-1 Conversion sequence mode select
- 00 Single-channel, single-conversion
- 01 Sequence-of-channels
- 10 Repeat-single-channel
- 11 Repeat-sequence-of-channels

ADC12BUSY Bit 0 ADC12 busy. This bit indicates an active sample or conversion operation.
- 0 No operation is active.
- 1 A sequence, sample, or conversion is active.

변환 완료 상태

ADC12MCTLx: memory control reg.

ADC12MCTLx, ADC12 Conversion Memory Control Registers

7	6	5	4	3	2	1	0
EOS	SREFx			INCHx			
rw–(0)	rw–(0)	rw–(0)	rw–(0)	rw–(0)	rw–(0)	rw–(0)	rw–(0)

Modifiable only when ENC = 0

EOS Bit 7 End of sequence. Indicates the last conversion in a sequence.
- 0 Not end of sequence
- 1 End of sequence

SREFx Bits 6-4 Select reference
- 000 $V_{R+} = AV_{CC}$ and $V_{R-} = AV_{SS}$
- 001 $V_{R+} = V_{REF+}$ and $V_{R-} = AV_{SS}$
- 010 $V_{R+} = Ve_{REF+}$ and $V_{R-} = AV_{SS}$
- 011 $V_{R+} = Ve_{REF+}$ and $V_{R-} = AV_{SS}$
- 100 $V_{R+} = AV_{CC}$ and $V_{R-} = V_{REF-}/ Ve_{REF-}$
- 101 $V_{R+} = V_{REF+}$ and $V_{R-} = V_{REF-}/ Ve_{REF-}$
- 110 $V_{R+} = Ve_{REF+}$ and $V_{R-} = V_{REF-}/ Ve_{REF-}$
- 111 $V_{R+} = Ve_{REF+}$ and $V_{R-} = V_{REF-}/ Ve_{REF-}$

INCHx Bits 3-0 Input channel select
- 0000 A0
- 0001 A1
- 0010 A2
- 0011 A3
- 0100 A4
- 0101 A5
- 0110 A6
- 0111 A7
- 1000 Ve_{REF+}
- 1001 V_{REF-}/Ve_{REF-}
- 1010 Temperature sensor
- 1011 $(AV_{CC} – AV_{SS}) / 2$
- 1100 $(AV_{CC} – AV_{SS}) / 2$, A12 on 'FG43x and 'FG461x devices
- 1101 $(AV_{CC} – AV_{SS}) / 2$, A13 on 'FG43x and 'FG461x devices
- 1110 $(AV_{CC} – AV_{SS}) / 2$, A14 on 'FG43x and 'FG461x devices
- 1111 $(AV_{CC} – AV_{SS}) / 2$, A15 on 'FG43x and 'FG461x devices

MSP430 ADC의 구별/특징
- 16개 메모리 각각에 대해 각자 기준전압 및 입력채널을 설정할 수 있다.
- 이는 4개 동작 모드(싱글채널–단일/반복 변환, 여러 채널–단일/반복 변환) 제공 가능하게 함.

ADC12MEMx, ADC12 Conversion Memory Registers

15	14	13	12	11	10	9	8
0	0	0	0	Conversion Results			
r0	r0	r0	r0	rw	rw	rw	rw

7	6	5	4	3	2	1	0
Conversion Results							
rw	rw	rw	rw	rw	rw	rw	rw

Conversion Results Bits 15-0 The 12-bit conversion results are right-justified. Bit 11 is the MSB. Bits 15-12 are always 0. Writing to the conversion memory registers will corrupt the results.

ADC12 관련 인터럽트

- MSP430xG461x 시리즈는 ADC12 관련 maskable irq. Vector를 가짐.

USCI_A0/USCI_B0 Transmit	UCA0TXIFG, UCB0TXIFG (see Note 1)	Maskable	0FFF0h	24
ADC12	ADC12IFG (see Notes 1 and 2)	Maskable	0FFEEh	23
Timer_A3	TACCR0 CCIFG0 (see Note 2)	Maskable	0FFECh	22
Timer_A3	TACCR1 CCIFG1 and TACCR2 CCIFG2, TAIFG (see Notes 1 and 2)	Maskable	0FFEAh	21
I/O Port P1 (Eight Flags)	P1IFG.0 to P1IFG.7 (see Notes 1 and 2)	Maskable	0FFE8h	20
USART1 Receive	URXIFG1	Maskable	0FFE6h	19
USART1 Transmit	UTXIFG1	Maskable	0FFE4h	18

- 여기서 ADC12IFG는 모두 18개의 인터럽트 사건(소스)들의 합성(ORed) 결과임. (즉 P1/2와 동일)
- 18개 irq. 소스도 다시 우선순위를 가짐
  - ADC12MEMx overflow: highest
  - ADC12MEM15 IFG: lowest

Irq. 관련 SFR:ADC12IV, ADC12IE/IFG

ADC12IV, ADC12 Interrupt Vector Register

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
r0	r0	r0	r0	r0	r0	r0	r0

7	6	5	4	3	2	1	0
0	0	ADC12IVx					0
r0	r0	r–(0)	r–(0)	r–(0)	r–(0)	r–(0)	r0

ADC12IVx Bits 15-0 ADC12 interrupt vector value

ADC12IV Contents	Interrupt Source	Interrupt Flag	Interrupt Priority
000h	No interrupt pending	–	
002h	ADC12MEMx overflow	–	Highest
004h	Conversion time overflow	–	
006h	ADC12MEM0 interrupt flag	ADC12IFG0	
008h	ADC12MEM1 interrupt flag	ADC12IFG1	
00Ah	ADC12MEM2 interrupt flag	ADC12IFG2	
00Ch	ADC12MEM3 interrupt flag	ADC12IFG3	
00Eh	ADC12MEM4 interrupt flag	ADC12IFG4	
010h	ADC12MEM5 interrupt flag	ADC12IFG5	
012h	ADC12MEM6 interrupt flag	ADC12IFG6	
014h	ADC12MEM7 interrupt flag	ADC12IFG7	
016h	ADC12MEM8 interrupt flag	ADC12IFG8	
018h	ADC12MEM9 interrupt flag	ADC12IFG9	
01Ah	ADC12MEM10 interrupt flag	ADC12IFG10	
01Ch	ADC12MEM11 interrupt flag	ADC12IFG11	
01Eh	ADC12MEM12 interrupt flag	ADC12IFG12	
020h	ADC12MEM13 interrupt flag	ADC12IFG13	
022h	ADC12MEM14 interrupt flag	ADC12IFG14	
024h	ADC12MEM15 interrupt flag	ADC12IFG15	Lowest

ADC12IE, ADC12 Interrupt Enable Register

15	14	13	12	11	10	9	8
ADC12IE15	ADC12IE14	ADC12IE13	ADC12IE12	ADC12IE11	ADC12IE10	ADC12IE9	ADC12IE8
rw–(0)	rw–(0)	rw–(0)	rw–(0)	rw–(0)	rw–(0)	rw–(0)	rw–(0)

7	6	5	4	3	2	1	0
ADC12IE7	ADC12IE6	ADC12IE5	ADC12IE4	ADC12IE3	ADC12IE2	ADC12IE1	ADC12IE0
rw–(0)	rw–(0)	rw–(0)	rw–(0)	rw–(0)	rw–(0)	rw–(0)	rw–(0)

ADC12IEx Bits 15-0 Interrupt enable. These bits enable or disable the interrupt request for the ADC12IFGx bits.
0 Interrupt disabled
1 Interrupt enabled

ADC12IFG, ADC12 Interrupt Flag Register

15	14	13	12	11	10	9	8
ADC12 IFG15	ADC12 IFG14	ADC12 IFG13	ADC12 IFG12	ADC12 IFG11	ADC12 IFG10	ADC12 IFG9	ADC12 IFG8
rw–(0)	rw–(0)	rw–(0)	rw–(0)	rw–(0)	rw–(0)	rw–(0)	rw–(0)

7	6	5	4	3	2	1	0
ADC12 IFG7	ADC12 IFG6	ADC12 IFG5	ADC12 IFG4	ADC12 IFG3	ADC12 IFG2	ADC12 IFG1	ADC12 IFG0
rw–(0)	rw–(0)	rw–(0)	rw–(0)	rw–(0)	rw–(0)	rw–(0)	rw–(0)

ADC12IFGx Bits 15-0 ADC12MEMx Interrupt flag. These bits are set when corresponding ADC12MEMx is loaded with a conversion result. The ADC12IFGx bits are reset if the corresponding ADC12MEMx is accessed, or may be reset with software.
0 No interrupt pending
1 Interrupt pending

Example code: polling method for ADC

```
void main(void)
{


//setup ADC12 for internal temp. sensor
  // Tsensor -- A10 channel
  // Vref =1.5V, tsample >=64 for(6MHz)
  ADC12CTL0 = REFON + SHT1_8 + ADC12ON;
  //conversion memory 0, single channel single conv., pulse mode,
  ADC12CTL1 = CSTARTADD_0 | SHS_0 | SHP | ADC12SSEL_0 | ADC12DIV_0 |
     CONSEQ_0;
  // conversion memory 0, Vref+, AVss, channel=10
  ADC12MCTL0 = EOS | SREF_0 | INCH_11;

ADC12CTL0 |= ADC12SC;
  while( ADC12CTL1 & ADC12BUSY ) ; //if busy, wait

  //read result value
  temperature = ADC12MEM0;
}
```