2011년2학기
임베디드시스템 응용(#514118)

#2. 78K0/KF2 Intro & GPIO

한림대학교
전자공학과 이선우

한림대학교
HALLYM UNIVERSITY

순 서

- 78K0/Kx2 series 소개
  - Features
  - Series lineup
- Port functions
  - Overview
  - Configuration
  - Control registers
  - Example codes

78K0/Kx2 Features

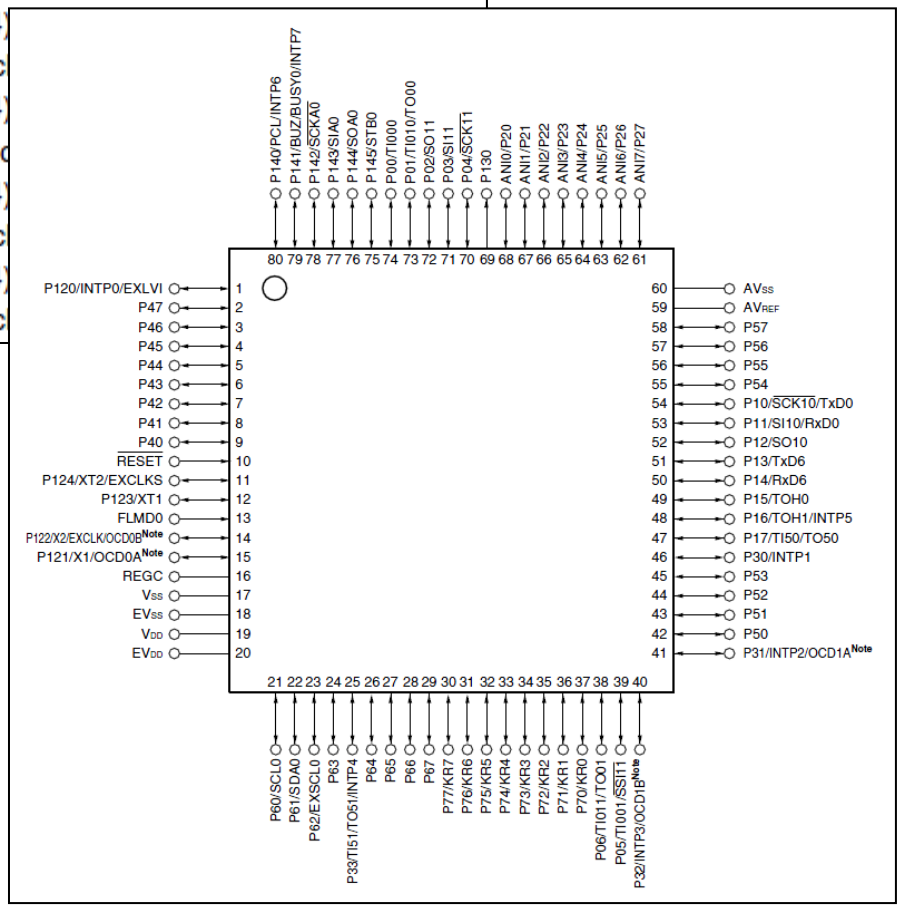
- 넓은 범위의 clock speed 지원: 122us@32768Hz~0.1us@20MHz
- General purpose registers: 8bitsX32
- Memory capacity
  - Program mem.(ROM): Flash 48K~128KB
  - Data mem.(RAM): Internal High-speed RAM 1KB, Internal Expansion RAM 1K~6KB
- On-chip peripherals
  - power-on-clear(POC), low-voltage detector(LVI), multiplier/divider (16X16, 32/16)
  - GPIO: 71 (N-ch open drain:4)
  - 8channels Timers
  - Serial interface: 5 channels;UART, CSI, I^2C
  - 10-bit ADC: 8 channels

Applications

- Automotive equipment
  - Sub-MCU for control
  - Car audio
- AV equip., home audio
- Household equip.
  - air conditioners, microwave ovens, etc.
- Industrial equip.
  - Pumps
  - Vending machines
  - Factory Automation

Name/Pin configuration

Part Number	Package	Quality Grade
μPD78F0544GC-UBT-A	80-pin plastic LQFP (14 × 14)	Standard
μPD78F0544GK-8EU-A	80-pin plastic LQFP (fine pitch) (12 × 12)	Standard
μPD78F0545GC-UBT-A	80-pin plastic LQFP (14 × 14)	
μPD78F0545GK-8EU-A	80-pin plastic LQFP (fine pitc	
μPD78F0546GC-UBT-A	80-pin plastic LQFP (14 × 14)	
μPD78F0546GK-8EU-A	80-pin plastic LQFP (fine pitc	
μPD78F0547GC-UBT-A	80-pin plastic LQFP (14 × 14)	
μPD78F0547GK-8EU-A	80-pin plastic LQFP (fine pitc	
μPD78F0547DGC-UBT-A[Note1]	80-pin plastic LQFP (14 × 14)	
μPD78F0547DGK-8EU-A[Note1]	80-pin plastic LQFP (fine pitc	



한림대학교 HALLYM UNIVERSITY

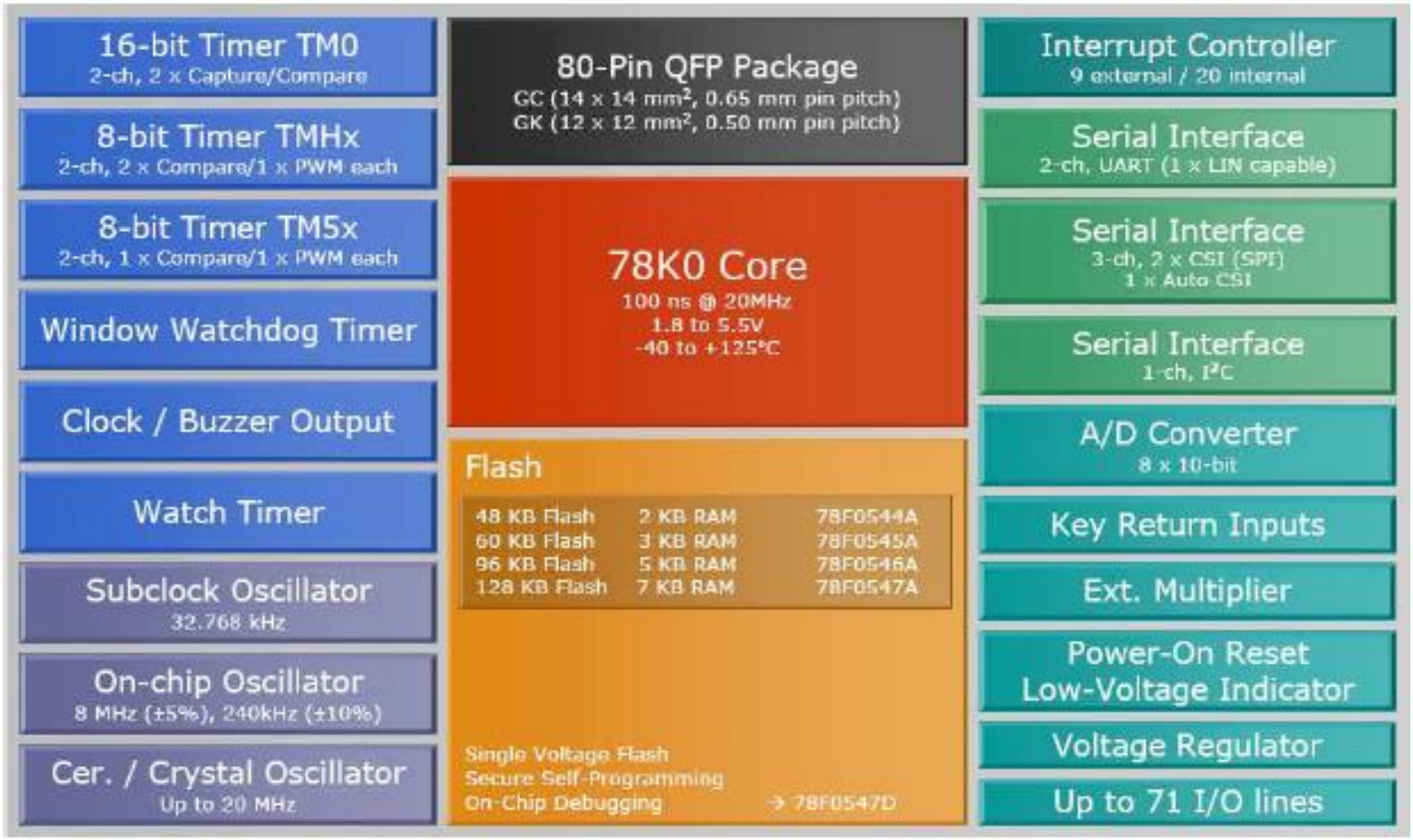
78K0/Kx2 series lineup

1.5 78K0/Kx2 Series Lineup

ROM	RAM	78K0/KB2	78K0/KC2		78K0/KD2	78K0/KE2	78K0/KF2
		30 Pins	44 Pins	48 Pins	52 Pins	64 Pins	80 Pins
128 KB	7 KB	–	–	–	μPD78F0527D[Note]	μPD78F0537D[Note]	μPD78F0547D[Note]
					μPD78F0527	μPD78F0537	μPD78F0547
96 KB	5 KB	–	–	–	μPD78F0526	μPD78F0536	μPD78F0546
60 KB	3 KB	–	–	μPD78F0515D[Note]	μPD78F0525	μPD78F0535	μPD78F0545
				μPD78F0515			
48 KB	2 KB	–	–	μPD78F0514	μPD78F0524	μPD78F0534	μPD78F0544
32 KB	1 KB	μPD78F0503D[Note]	μPD78F0513D[Note]	μPD78F0513	μPD78F0523	μPD78F0533	–
		μPD78F0503	μPD78F0513				
24 KB	1 KB	μPD78F0502	μPD78F0512		μPD78F0522	μPD78F0532	–
16 KB	768 B	μPD78F0501	μPD78F0511		μPD78F0521	μPD78F0531	–
8 KB	512 B	μPD78F0500	–		–	–	–

Note Product with on-chip debug function

Block diagram



한림대학교 HALLYM UNIVERSITY

CH. 5
PORT FUNCTION

GPIO Overview

- Total 71 I/O lines (CMOS I/O:66, O:1, open-drain I/O:4)
  - P0:P00~P06 (7-bit I/O), on-chip pull-up circuit 지원
  - P1, P4, P5, P7: 8-bit I/O, pull-up 지원
  - P2:8bit I/O, ADC input0~7
  - P3:4bit I/O, external input (INTP1~4)
  - P6: P60~P63; N-ch open drain output, P64~P67: 4bit I/O
  - P12:5bit I/O, only P120 use pull-up circuit.
  - P13:P130; 1bit output only port
  - P14:6bit I/O

Related control registers

- 4 종류의 레지스터에 의해 각 핀의 역할 결정됨
  - Port Mode reg. (PM0~PM7, PM12, PM14)
    - 개별 핀(포트)의 direction(Input/output) 결정.
    - 1=input, 0=output
    - Reset 후엔 모두 0xFF (In mode)
  - Port reg. (P0~P7, P12, P14)
    - Output mode에선 각 핀의 출력(H/L) 결정
    - Input mode에선 각 핀의 level에 따라 1/0 결정됨.
    - Reset 후엔 0x00
  - Pull-up resistor option reg. (PU0,PU1,PU3~PU7, PU12, PU14)
    - 각 핀의 내부 풀업 저항 연결 여부 결정: 1=연결,0=사용하지 않음.
  - A/D port configuration reg. (ADPC)
    - P2의 경우 ANI0~ANI7과 동시 기능. 따라서 이 레지스터 값에 따라 ADC input으로 사용 가능

Example codes

```
//앞 부분 생략
//Port setup
//P24~P27:input, P20~P23: output
  PM2 = 0x0f;
//P5: 8비트 모두 출력으로 설정
  PM5 = 0;

//P2의 상위 4비트를 읽어 P5하위 4비트로
출력
  P5 = (P2 & 0xf0)>>4;
```

실습 보드 GPIO 관련 주변 장치

- CPU board
  - Digital output: 7segment →P5 연결
  - Digital input: external input 2 lines (INTP0/1)
- Main board
  - Digital outputs: 4 LEDs → P04, P12, P43, P67
  - Digital inputs:4 slide switches (P24~P27), 4X4 matrix keypad (P7)
  - 8X8 dot matrix LED array를 사용하려면 CPU 보드의 하드웨어를 수정해야 한다. (학기 프로젝트에서는 사용 가능)